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BIFOCAL SCIENCE

Strictly As per HSC Board Syllabus of Higher Secondary Education

Prof. Sharad S. Wagh

M. Tech. (EXTC)

Head of Electronics and Telecommunication Engineering Dept.

Vishwaniketan's Institute of Management Entrepreneurship & Engineering Technology,

Kumbhivali, Tal. - Khalapur, Maharashtra - 410202 India.

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Preface

Dear Student,

We are extremely happy to present the book of "**Computer Science – II**" for you. The topics within the chapters have been arranged in a proper sequence to ensure smooth flow of the subject.

Salient Features of the Book are as follows :

1. Selective Board Examination Questions till March 2023 have been fully solved in this edition.

2. Theory is accompanied with neat & clean figures.

3. MCQ's with explanation are also included at the end of each chapter. The latest trend in education is the teaching through multiple choice questions. The MCQ's are intended to enable students to prioritise and plan their learning through regular practice. The book contains large number of multiple choice questions on the subject.

4. Each chapter is divided into various sections and sub-sections. Entire syllabus is divided into Chapters, sections and headings. Each paragraph has been given a unique section/subsection number which is used to explain that particular section for the students as a cross reference to enable them to refer to the related paragraph.

5. Through this book, the author has made an effort to provide rationale for the solutions. The book, therefore, meets the expectations of the students as it answers the demand and the quest in their mind. It would give rise to real learning which would stand in good stead for the student's career and his life.

6. The book is user-friendly and provides information in a well structured manner. It provides comprehensive and critical study of the various concepts of the subject matter. It is felt that the contents should be crystal clear.

7. **Programs are made simple & Outputs are displayed.**

A word or suggestion from your side may help us add another feather to the cap of the subject matter of the book. The author looks forward to the comments, suggestions and criticism from the readers. Constructive suggestions and feedback from users would be highly appreciated, acknowledged and suitably incorporated

We are thankful to team of Target Publications and Tech Neo Publications for the encouragement and support that they have extended to us.

- Authors

Syllabus

STD. XII - S.Y.J.C. (Science)

Computer Science - II

1. Introduction to Microprocessors & Organization of 8085

Evolution of Microprocessor, What is Microprocessor? Block diagram of Generic Microprocessor and study of various blocks in it. Block Diagram of 8085 µp. Study of various blocks and functions of various pins on it. **(Refer Chapter 1)**

2. Instruction Set and Programming Of 8085

Addressing Modes in 8085, Programming mode of 8085. Study of Instruction Set - Data transfer, Arithmetic, Logic, Branching, Stack, I/O and Machine Control Group Instructions. Assembly language programs based on above instructions. (**Note:** The program size generally should not exceed 20-25 instructions). **(Refer Chapter 2)**

3. Introduction to Intel X86 Family

Introduction to Advance Microprocessors, Introduction to X86 Family and study of major attributes of the X86 family processors, Programming Model of X86 family of microprocessors.

(Refer Chapter 3)

4. Introduction to Microcontroller

Introduction to Microcontroller, Study of 8051 Architecture and Programming model, Overview of other Microcontroller's in the 8051 family. Application of Microcontroller.

(Refer Chapter 4)

5. Networking Technology

Study of transmission media - Cable media. Coaxial. Twisted pair. Fiber optic. Their comparison. Introduction to wireless media. Network topologies - Access methods, Topologies - Bus, Ring, Star, Ethernet, Token ring, Protocols - Internet protocol, Introduction to connectivity devices - Modem, Hubs, Repeaters and Routers. **(Refer Chapter 5)**

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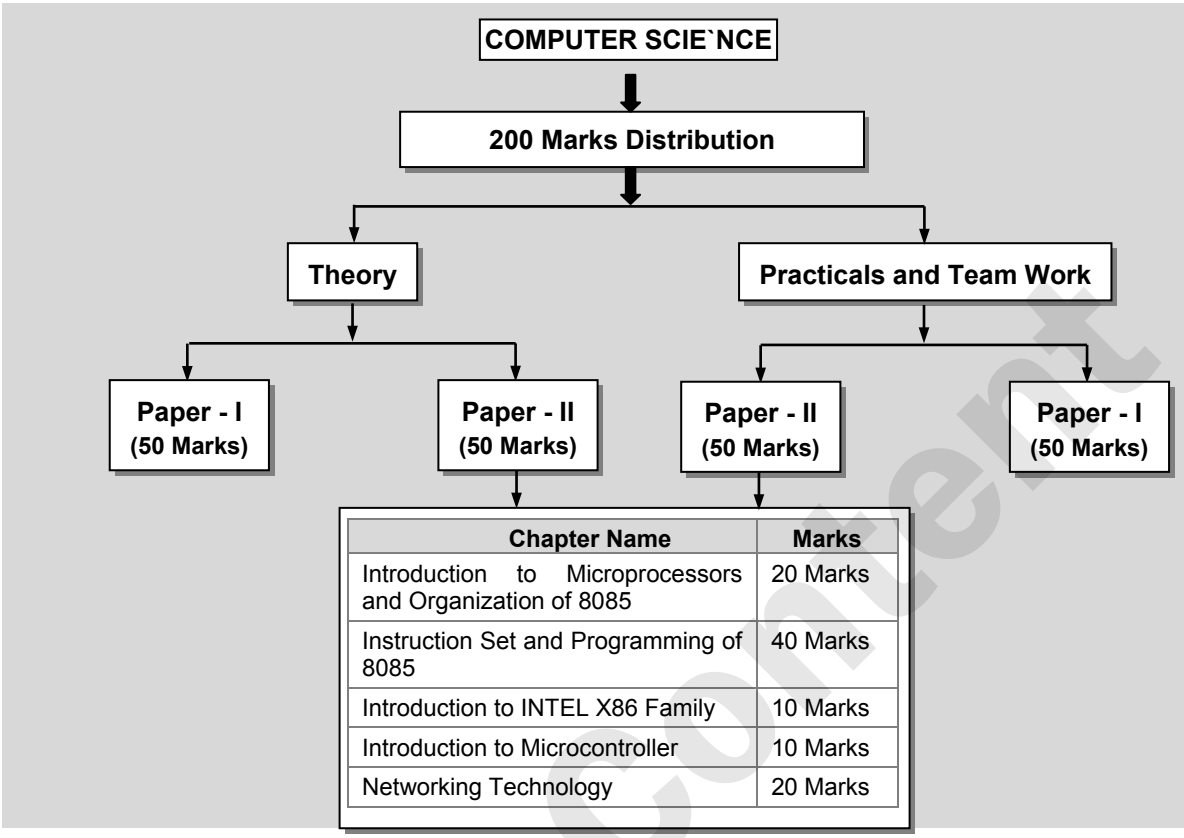

Chapter Name	Marks
Introduction to Microprocessors and Organization of 8085	20 Marks
Instruction Set and Programming of 8085	40 Marks
Introduction to INTEL X86 Family	10 Marks
Introduction to Microcontroller	10 Marks
Networking Technology	20 Marks

Question Paper Format

Each Question Paper will have Five Main Questions

Q. 1(A)	4 MCQs - 1 Mark each (Compulsory)	4 Marks
Q. 1(B)	**(a)** - 3 Marks **(b)** - 3 Marks **(c) -** 3 Marks *(Attempt any Two)*	6 Marks
Q. 2(A)	**(a)** - 3 Marks **(b)** - 3 Marks **(c)** - 3 Marks *(Attempt any Two)*	6 Marks
Q. 2(B)	**(a)** - 4 Marks **(b)** - 4 Marks *(Attempt any One)*	4 Marks
Q. 3(A)	**(a)** - 3 Marks **(b)** - 3 Marks **(c)** - 3 Marks *(Attempt any Two)*	6 Marks
Q. 3(B)	**(a)** - 4 Marks **(b)** - 4 Marks *(Attempt any One)*	4 Marks
Q. 4(A)	**(a)** - 3 Marks **(b)** - 3 Marks **(c)** - 3 Marks *(Attempt any Two)*	6 Marks
Q. 4(B)	**(a)** - 4 Marks **(b)** - 4 Marks *(Attempt any One)*	4 Marks
Q. 5	**(a)** - 5 Marks **(b)** - 5 Marks **(c)** - 5 Marks *(Attempt any Two)* **OR**	10 Marks
Q. 5	**(a)** - 5 Marks **(b)** - 5 Marks **(c)** - 5 Marks *(Attempt any Two)*	10 Marks
	Total :	**50 Marks**

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Chapter 5 : Networking Technology 5-1 to 5-42

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CHAPTER

3

Introduction to INTEL X86 Family

3.1 INTRODUCTION TO ADVANCE MICROPROCESSOR

An advanced microprocessor refers to a h**igh-performance and feature-rich microprocessor** that incorporates advanced technologies and architectural improvements to deliver superior processing capabilities. These processors are designed to handle complex tasks and demanding applications with enhanced efficiency, speed, and functionality.

3.1.1 Characteristics of Advanced Microprocessors

1. **Increased Performance :** Advanced microprocessors are designed to offer higher clock speeds and improved instruction execution capabilities. They employ advanced pipelining techniques, superscalar architectures, and multiple execution units to achieve greater performance levels.
2. **Expanded Instruction Set:** These microprocessors typically have an expanded **instruction set architecture (ISA)** that includes a wide range of specialized instructions for advanced operations. These instructions can accelerate mathematical computations, multimedia processing, encryption/decryption, and other complex tasks.
3. **Enhanced Cache and Memory Hierarchy :** Advanced microprocessors incorporate larger and faster on-chip caches, such as L1, L2, and sometimes L3 caches. These caches help reduce memory access latency and improve overall system performance. They also employ sophisticated memory management techniques like virtual memory and caching algorithms to optimize data access.
4. **Multithreading and Parallel Processing :** To improve system responsiveness and utilization of available resources, advanced microprocessors often support multithreading and parallel processing techniques. These processors can execute multiple threads simultaneously or perform parallel computations using multiple cores or execution units.
5. **Advanced Power Management :** Power efficiency is a critical consideration in modern microprocessor design. Advanced microprocessors employ advanced power management techniques, such as **dynamic voltage and frequency scaling (DVFS)**, power gating, and clock gating, to reduce power consumption during periods of low activity or idle states.
6. **Integrated Peripheral Interfaces :** Many advanced microprocessors feature integrated peripherals and interfaces, such as USB, Ethernet, SATA, PCIe, and graphics controllers. These integrated features simplify system design, reduce costs, and enhance overall system performance.
7. **Security Features :** Security is a significant concern in modern computing environments. Advanced microprocessors often incorporate hardware-level security features like encryption/decryption accelerators, secure boot mechanisms, and hardware-based security modules to ensure data protection and system integrity.

3.2 BASICS OF 8086 (16-BIT MICROPROCESSOR)

i. The 8086 microprocessor is a **16-bit microprocessor** that was introduced by Intel in 1978. It is considered one of the first microprocessors to have a significant impact on the personal computer industry.

ii. The 8086 was the first member of the x86 family of microprocessors, which has since become the most widely used architecture in the PC market.

iii. The 8086 microprocessor was a significant advancement over its predecessors in terms of performance and capabilities.

iv. It has a 16-bit architecture, which means it could process data in 16-bit chunks, allowing for larger memory addressing and more complex calculations compared to the 8-bit processors of the time.

3.2.1 Features of 8086 Microprocessor

i. It is a 16-bit µp.

ii. 8086 has a 20-bit address bus can access up to 220 = 10, 48,576 memory locations approximately 1 MB of Memory Space.

iii. 8086 has a 16-bit Data bus can support up to 216 = 65,536 I/O ports.

iv. It provides 14, 16 -bit registers.

v. It has multiplexed address and data bus AD0 - AD15.

vi. 8086 available to works on 5 MHz, 8 MHz and 10 MHz

vii. It requires single phase clock with 33% duty cycle to provide internal timing.

viii. It can prefetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution.

ix. 8086 has pipelined architecture.

x. 8086 is designed to operate in two modes, Minimum and Maximum.

xi. It requires +5V power supply.

xii. A 40-pin dual in line package (DIP).

3.3 ARCHITECTURE OF 8086 (BLOCK DIAGRAM OF 8086)

i. 8086 has two blocks : BIU (Bus Interface Unit) and EU (Execution Unit).

a. The **BIU performs all bus operations** such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory operands.

b. The instruction bytes are transferred to the instruction queue. EU executes instructions from the instruction system byte queue.

c. **Both units operate asynchronously** to give the 8086 an overlapping instruction fetch and execution mechanism which is called as Pipelining. This results in efficient use of the system bus and system performance.

d. BIU contains Instruction queue, Segment registers, Instruction pointer, and Address adder.

e. EU contains Control circuitry, Instruction decoder, ALU, Pointer and Index register, Flag register.

f. The Architecture of 8086 is as shown in Fig 3.3.1.

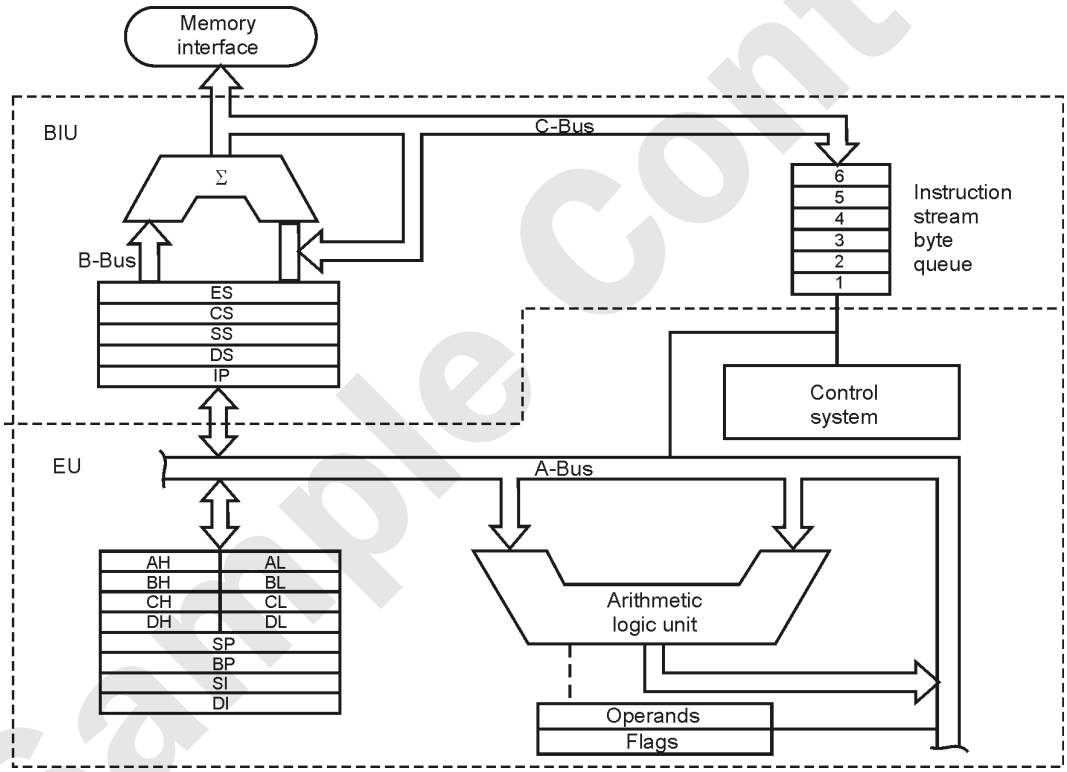

Fig. 3.3.1 : Internal Architecture of 8086

3.3.1 Bus Interface Unit (BIU)

i. It provides a full 16-bit bidirectional data bus and 20 bit address bus.

ii. The bus interface unit is responsible for performing all external bus operations. Specifically it has the following functions:

a. Instructions fetch.

b. Instruction queuing

c. Operand fetch and storage.

d. Address relocation and Bus control.

iii. BIU consist of 6 bytes of a QUEUE and Address Summer.

iv. The BIU uses a mechanism known as an instruction stream queue to implement pipeline architecture.

v. Fetching the next instruction while current instruction executes is known as Pipelining. This queue permits prefetch of up to six bytes of instruction code.

vi. Whenever the queue of the BIU is not full, it has room for at least two more bytes and at the same time the EU is not requesting it to read or write operands from memory, the BIU is free to look ahead in the program by prefetching the next sequential instruction.

vii. These prefetching instructions are held in its FIFO queue. With its **16 bit data bus**, the BIU fetches two instruction bytes in a single memory cycle.

viii. After a byte is loaded at the input end of the queue, it automatically shifts up through the FIFO to the empty location nearest the output.

ix. The EU accesses the queue from the output end. It reads one instruction byte after the other from the output of the queue. If the queue is full and the EU is not requesting access to operand in memory.

x. These intervals of no bus activity, which may occur between bus cycles, are known as idle state.

xi. If the BIU is already in the process of fetching an instruction when the EU request it to read or write operands from memory or I/O, the BIU first completes the instruction fetch bus cycle before initiating the operand read / write cycle.

xii. The BIU also contains a dedicated adder which is used to generate the 20bit physical address that is output on the address bus. This address is formed by adding an appended 16-bit segment address and a 16 bit offset address.

xiii. For example: The physical address of the next instruction to be fetched is formed by combining the current contents of the code segment CS register and the current contents of the instruction pointer IP register.

xiv. The BIU is also responsible for generating bus control signals such as those for memory read or write and I/O read or write.

The BIU contains the following registers:

a. IP - the Instruction Pointer

b. CS - the Code Segment Register

c. DS - the Data Segment Register

d. SS - the Stack Segment Register

e. ES - the Extra Segment Register

3.3.2 Execution Unit

i. The Execution unit is responsible for decoding and executing all instructions.

ii. The EU extracts instructions from the top of the queue in the BIU, decodes them, generates operands, if necessary, passes them to the BIU and requests it to perform the read or write cycles to memory or I/O and perform the operation specified by the instruction on the operands.

iii. During the execution of the instruction, the EU tests the status and control flags and updates them based on the results of executing the instruction.

iv. If the queue is empty, the EU waits for the next instruction byte to be fetched and shifted to top of the queue.

v. When the EU executes a branch or jump instruction, it transfers control to a location corresponding toanother set of sequential instructions.

vi. Whenever this happens, the BIU automatically resets the queue and then begins to fetch instructionsfrom this new location to refill the queue.

vii. 8086 provides 14, 16 –bit Registers

Registers are in the CPU and are referred to by specific names :

a. Data registers

1. Hold data for an operation to be performed
2. There are 4 data registers (AX, BX, CX, DX)

b. Address registers

1. Hold the address of an instruction or data element
2. Segment registers (CS, DS, ES, and SS)
3. Pointer registers (SP, BP, and IP)
4. Index registers (SI, DI)

c. Status register

1. Keeps the current status of the processor.
2. On an IBM PC the status register is called the FLAGS register.

viii. In total there are **fourteen 16-bit registers** in an 8086/8088.

3.3.3 Flag Register of 8086

Board Exam Question

Q. Explain X86 flag register with diagram ?

(March 16, Oct. 11, 4 Marks)

i. It determines the current state of the processor.

ii. It consists of 6 Conditional flags

a. Conditional flags are set according to some results of arithmetic operation.

b. Programmer do not allow to alter the value of these conditional flags.

1. Sign Flag (SF)
2. Zero Flag (ZF)
3. Auxiliary carry Flag (AF)
4. Parity Flag (PF)
5. Carry Flag (CF)
6. Overflow Flag (OF)

iii. It consists of **3 Control flags**

a. Control flags are used to control some operations of the Microprocessor.

b. These flags are tobe set by programmer in order to achieve some specific purposes.

1. Direction Flag (DF)
2. Interrupt-enable Flag (IF)
3. Single-step Flag (TF)

iv. Flag register is as shown if Fig. 3.3.2.

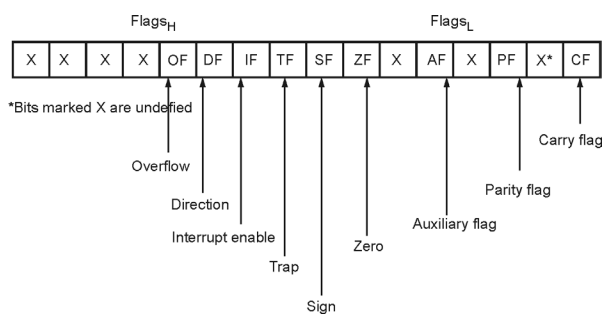

Fig. 3.3.2 : Flag Register of 8086

Conditional Flags of 8086

i. Sign Flag (SF)

a. Set if the most significant bit of the result is one.

b. Since negative binary numbers are represented using standard two's complement notation, the MSB (copied in sign flag) indicates the number is positive or negative.

c. SF indicates sign of the result only in case of signed operation.

d. SF = 1; Result is Negative

e. SF = '0'; Result is Negative

f. In case of unsigned operation, sign bit has no significance.

ii. Zero Flag (ZF)

a. After Arithmetical and Logical operation results in Zero, as a result the zero flag is set

b. It is not available for programmer for changing to Zero flag.

c. If a result is non zero then zero flag is reset

iii. Auxiliary carry Flag (AF)

a. This flag is **affected after addition only**. If there is a carry from D3 to D4 bit during an 8-bit addition, this bit is set otherwise this bit is reset.

b. If there is a carry from D7 to D8 bit during a 16-bit addition, this bit is set otherwise this bit is reset.

c. This is not a general flag; it is only used internally by microprocessor to perform binary to BCD conversion.

iv. Parity Flag (PF)

a. This flag is affected after Arithmetical and Logical operation. This flag is affected by number of 1's in an accumulator register.

b. If A register containing odd number of 1's then this flag is set, otherwise for number of 1's in A register is even then this bit is reset.

v. Carry Flag (CF)

a. If an operation performed in ALU generates a carry after 8-bit addition from D7 bit to next stage, the Cy flag is set. It works as 9th bit for addition & as Borrow flag for subtraction. If there is no carry borrow out of MSB bit i.e., D7 of the result the CY flag is reset.

b. If an operation performed in ALU generates a carry after 16-bit addition from D15 bit to next stage, the Cy flag is set. It works as 16^{th}bit for addition & as Borrow flag for subtraction. If there is no carry borrow out of MSB bit i.e., D15 of the result the CY flag is reset.

vi. Overflow Flag (OF)

a. In case of signed operations, it indicates that the result is outside the range (maximum or minimum representable number).

b. In case of unsigned operation, this bit is insignificant.

Control flags

i. Direction Flag (DF)

a. This flag supports string instructions of 8086. These are a special type of instructions that can work on an entire array of data.

b. Since single instruction can do the operation on an entire array of data, the time required to fetch and decode the instruction again and again will reduce drastically

c. If DF=1, then string manipulation instructions will auto-decrement index registers. If DF=0, then the index registers will be auto-incremented.

ii. Interrupt-enable Flag (IF)

a. 8086 has maskable as well as non-maskable interrupts. Interrupt Enable flag is used to **enable or disable the maskable interrupt.**

b. If IF=1, Interrupt Enable

c. If IF=0, Interrupt Disable

iii. Single-step Flag (TF)

a. This flag is used for debugging a program

b. If set then single-step interrupt will occur after the next instruction.

3.3.4 Register Organization of 8086 Microprocessor

Board Exam Question

Q. Draw and explain the programming model of 16-bit version of Intel X86 microprocessor family.

(March 05, 10, 14, 4 Marks)

i. 8086 provides 14, 16 -bit Registers

Registers are in the CPU and are referred to by specific names :

a. Data registers

1. Hold data for an operation to be performed
2. There are 4 data registers (AX, BX, CX, DX)

b. Address registers

1. Hold the address of an instruction or data element
2. Segment registers (CS, DS, ES, and SS)
3. Pointer registers (SP, BP, and IP)
4. Index registers (SI, DI)

c. Status register

1. Keeps the current status of the processor.
2. On an IBM PC the status register is called the FLAGS register.

ii. The Fig. 3.3.3 Shows the register section of 8086.

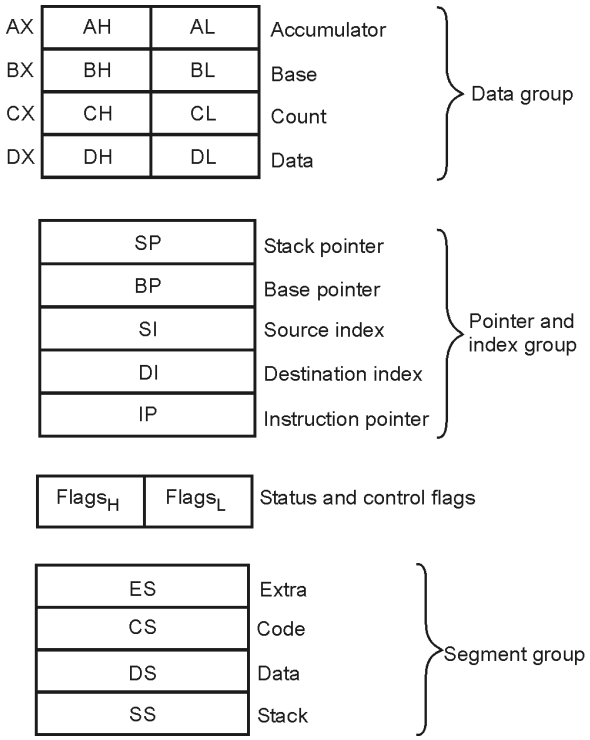

Fig. 3.3.3 : Register Section of 8086

General Purpose Registers or Data Registers (AX, BX, CX, DX)

i. Instructions execute faster if the data is in a register. AX, BX, CX, DX are the data registers. Low and High bytes of the data registers can be accessed separately.
ii. AH, BH, CH, DH are the high bytes registers. AL, BL, CL, and DL are the low bytes registers.
iii. Data Registers are general purpose registers but they also perform special functions

AX Register

i. It is Accumulator Register. Preferred register to use in arithmetic, logic and data transfer instructions because it generates the shortest Machine Language Code.
ii. Used in multiplication and division operations, also used in I/O operations.

BX Register

i. It is Base Register. Also serves as an address register.
ii. Used in array operations, Table Lookup operations (XLAT).

CX Register

i. It is Count register.
ii. Used as a loop counter, shift and rotate operations.

DX Register

i. It is Data register.
ii. Used in multiplication and division, and in arithmetic and other operations.
iii. It is also used in I/O operations.
iv. It Contains the offset addresses of memory locations.

Pointer and Index Registers (SP, BP, SI, DI)

i. Contains the offset addresses of memory locations.
ii. Can also be used in arithmetic and other operations.

SP(Stack pointer)

i. Used to hold the offset Address for stack segment by Default.
ii. It is used for Physical Address Generation.
iii. Used with SS to access the stack segment.

BP (Base Pointer)

i. Used to hold the offset Address for stack segment by Default.
ii. It is used for Physical Address Generation.
iii. Primarily used to access data on the stack.
iv. Can be used to access data in other segments.

SI (Source Index register)

i. Used to hold the offset Address for Data segment by Default.
ii. It is used for Physical Address Generation.
iii. Is required for some string operations.
iv. When string operations are performed, the SI register points to memory locations in the data segment which is addressed by the DS register. Thus, SI is associated with the DS in string operations.

DI (Destination Index register)

i. Used to hold the offset Address for Extra segment by Default.
ii. It is used for Physical Address Generation.
iii. Is also required for some string operations.
iv. When string operations are performed, the DI register points to memory locations in the data segment which is addressed by the ES register. Thus, DI is associated with the ES in string operations.

Segment Registers (CS, DS, ES, SS)

CS (Code Segment Register)

i. Used to hold the Base Address for Code segment.
ii. It is used for Physical Address Generation for Program Memory.
iii. Points at the segment containing the current program.

DS (Data Segment Register)

i. Used to hold the Base Address for Data segment.
ii. It is used for Physical Address Generation for Program Memory.
iii. Generally points at segment where variables are defined.

ES (Extra Segment Register)

i. Used to hold the Base Address for Extra segment.
ii. It is used for Physical Address Generation for Program Memory
iii. Extra segment register, it's up to a coder to define its usage.

SS (Stack Segment Register)

i. Used to hold the Base Address for Stack segment.
ii. It is used for Physical Address Generation for Temporary Memory.
iii. Points at the segment containing the stack.

Status registers (FLAG and IP)
IP (Instruction Pointer Register)

i. This is a crucially important register which is used to control which instruction the CPU executes.
ii. The IP program counter is used to store the memory location of the next instruction to be executed.
iii. The CPU checks the program counter to ascertain which instruction to carry out next. It then updates the program counter to point to the next instruction.
iv. Thus, the program counter will always point to the next instruction to be executed.

⏭ 3.4 80286 MICROPROCESSOR

i. The 80286, also known as the Intel 286, is a microprocessor that was released by Intel in 1982.
ii. It was the successor to the popular 8086 and 8088 processors.
iii. The 80286 represented a significant improvement over its predecessors and introduced several new features.

3.4.1 Features and Characteristics of the 80286

16-bit Architecture

i. The 80286 is a 16-bit microprocessor, which means it operates on data and instructions in 16-bit data.
ii. This allowed for more efficient processing and improved performance compared to 8-bit processors.

Protected Mode

i. The 80286 introduced a new operating mode called "**Protected Mode.**"
ii. In this mode, the processor had the ability to address up to 16MB of memory and offered memory protection, allowing multiple programs to run simultaneously without interfering with each other's memory space.

Real Mode

The 80286 also supported the traditional "**Real Mode**" of operation, which was backward compatible with the 8086 and 8088 processors. In Real Mode, the processor could only address up to 1MB of memory and did not provide memory protection.

Virtual 8086 Mode

i. Another notable feature of the 80286 was the introduction of the "Virtual 8086 Mode."
ii. This mode allowed the processor to run multiple real mode programs concurrently within protected mode, providing a level of compatibility for older software.

Increased Performance

The 80286 offered a significant performance improvement over its predecessors. It had a higher clock speed, improved instruction set, and a more efficient memory management system. These enhancements made it popular for running multitasking operating systems and more demanding applications.

External Coprocessor Support

i. The 80286 introduced support for an external math coprocessor (known as the 80287) that provided enhanced floating-point arithmetic capabilities.
ii. The coprocessor improved the performance of mathematical and scientific applications.
iii. Despite its advancements, the 80286 had some limitations. For instance, it lacked a built-in memory management unit (MMU), requiring an external MMU to be used in protected mode.
iv. It also had limited instruction set capabilities compared to later processors like the 80386.
v. The 80286 played a crucial role in the evolution of x86 processors and laid the foundation for the subsequent generations of Intel processors.
vi. It was widely used in personal computers, workstations, and early server systems, but has since been surpassed by more powerful and advanced processors.

⏭ 3.5 80386 MICROPROCESSOR

Board Exam Question

Q. List the advanced microprocessor of INTEL X86 family and mention three attributes of anyone of them. **(Oct. 03, 3 Marks)**

i. The 80386, often referred to as the Intel 386 or simply the 386, is a microprocessor chip introduced by Intel in 1985.
ii. It is part of the x86 family of microprocessors and is a significant advancement over its predecessor, the Intel 80286.
iii. The 80386 brought several important features and improvements to the x86 architecture.

Features and characteristics of the 80386

32-bit Architecture

The 80386 introduced a 32-bit instruction set architecture, which allowed it to process data and instructions in 32-bit data's, significantly increasing the amount of memory it could access.

Protected Mode

i. The 386 introduced a protected mode, which provided improved memory management and multitasking capabilities.
ii. It allowed the processor to run multiple applications simultaneously and protected them from interfering with each other's memory spaces.

Virtual 8086 Mode

i. The virtual 8086 mode allowed the 386 to run legacy 16-bit software designed for earlier x86 processors.
ii. It provided a compatibility layer for running older DOS applications within a protected mode environment.

Enhanced Performance

i. The 386 offered improved performance compared to its predecessors.
ii. It had a larger instruction cache, a faster memory interface, and a more efficient bus architecture, resulting in faster execution of instructions and increased overall performance.

Increased Addressable Memory

i. The 386 could address up to **4 gigabytes (4GB)** of physical memory, significantly more than the 16MB limit of the 80286.
ii. This expanded memory capacity was particularly beneficial for demanding applications and operating systems.

Integrated Math Coprocessor

i. Some versions of the 386, such as the 80386DX, included an integrated math coprocessor (known as the 80387).
ii. The coprocessor provided hardware acceleration for floating-point arithmetic, improving performance in mathematical and scientific computations.
iii. The Intel 80386 was a landmark microprocessor that played a crucial role in the evolution of personal computing.
iv. Its advanced features and increased performance capabilities set the stage for future x86 processors and helped pave the way for modern computing systems.

⏭ 3.6 80486 MICROPROCESSOR

i. The 80486, commonly known as the Intel 486 or simply the 486, is a microprocessor introduced by Intel in 1989.
ii. It is part of the x86 family of processors and is the successor to the Intel 386 processor.
iii. The 80486 was a significant step forward in terms of performance compared to its predecessor. It introduced several architectural enhancements and improvements over the 386, including an on-chip unified instruction and data cache, an integrated **floating-point unit (FPU),** and a **built-in memory management unit (MMU)**.
iv. These features contributed to faster processing speeds and improved overall system performance.
v. The 486 was available in various clock speeds, ranging from **25 MHz to 100 MHz,** with later models reaching speeds up to 150 MHz.
vi. It supported a 32-bit architecture and offered improved performance for both general-purpose computing tasks and multimedia applications.
vii. One notable feature of the 486 is that it popularized the use of the Socket 1 and Socket 2 designs, which allowed for easy upgrades by simply swapping out the processor. This made it a popular choice for many PC users at the time.
viii. The 80486 had a significant impact on the computing industry and played a crucial role in the evolution of personal computers. Its performance and capabilities contributed to advancements in areas such as gaming, graphics, and software development.
ix. It's important to note that the 80486 is now considered an outdated processor, and it has been succeeded by several generations of processors, including the Pentium, Core, and the more recent Intel Core i series.

⏭ 3.7 80586 OR PENTIUM MICROPROCESSOR

Board Exam Questions

Q. List and explain any four prominent main features of Pentium processor.
(March 07, 11, 15, Oct. 04, 09,14 3/4 Marks)

Q. Explain the following terms of advance X86 family microprocessors :
(i) Branch prediction (ii) Dual pipeline
(iii) 64 bit data bus (iv) On chip cache
(March 06, 10, 13, 16, Oct. 08, 10, 15, 3/4 Marks)

i. The term "80586" refers to the microprocessor architecture developed by Intel, commonly known as the Pentium processor.
ii. The Intel 80586 is an x86-based CPU that was introduced as the successor to the Intel 80486 processor.
iii. The name "Pentium" was later adopted as the official brand name for Intel's fifth-generation microprocessors.
iv. The naming convention for Intel's processors moved away from the model numbers like "80586" and instead adopted names like Pentium, Pentium II, Pentium III, and so on.

Features and characteristics of the 80586 (Pentium Processor)

i. **Architecture :** The Pentium processors are based on the x86 architecture, which is the foundation of most desktop and laptop computers.
ii. **Clock Speed :** Pentium processors were available in a range of clock speeds, starting from around 60 MHz and gradually increasing with newer generations.

iii. **Instruction Set :** The Pentium processors introduced several new instructions to enhance performance and enable more advanced features.

iv. **Pipelining :** Pentium processors implemented a superscalar architecture with multiple execution units, allowing them to execute multiple instructions simultaneously.

v. **Floating-Point Performance :** Pentium processors introduced an improved floating-point unit, which enhanced their ability to perform mathematical calculations.

vi. **Cache :** Pentium processors featured larger and faster on-chip caches compared to their predecessors, which helped reduce memory latency and improve performance.

vii. **MMX Technology :** Later iterations of the Pentium processors introduced MMX (Multi-Media Extensions) technology, which provided enhanced multimedia capabilities, such as faster video and audio processing.

viii. **Bus Architecture :** The Pentium processors utilized a 32-bit system bus known as the Front Side Bus (FSB) to communicate with other components in the computer system.

ix. **Overclocking :** Some Pentium processors were popular for their overclocking potential, allowing users to increase the clock speed beyond the manufacturer's specifications for additional performance.

x. **Compatibility :** Pentium processors were designed to be backward compatible with previous generations of x86 processors, ensuring software compatibility with a wide range of applications and operating systems.

3.7.1 Advantages of 80586 or Pentium Microprocessor

Board Exam Question

Q. Explain the advantages of following features of Pentium processor : (i) Prefetching (ii) Internal data bus. **(March 16, 2 Marks)**

I. Prefetching

Prefetching is a feature in Pentium processors that helps improve performance by fetching data and instructions from memory in advance and storing them in a cache. Here are the advantages of prefetching:

Reduced memory latency

i. Prefetching allows the processor to anticipate future data and instruction needs and fetch them in advance. By doing so, it reduces the time required to access data from the main memory, which can be a relatively slow operation.

ii. This helps to minimize memory latency and improves overall system performance.

Increased instruction execution

i. Prefetching enables the processor to fetch and store instructions ahead of time.

ii. This ensures a steady supply of instructions to the execution unit, reducing potential instruction bottlenecks and increasing the processor's ability to execute instructions quickly.

Efficient resource utilization

i. By prefetching data and instructions in advance, the Pentium processor can make more efficient use of its resources.

ii. It can overlap the fetching and execution of instructions, reducing idle time and maximizing the utilization of execution units.

Enhanced branch prediction

i. Prefetching also plays a role in improving branch prediction accuracy.

ii. The processor can anticipate and prefetch instructions along predicted branch paths, reducing the impact of branch mispredictions and improving overall instruction throughput.

II. Internal data bus

i. The internal data bus, also known as the system bus or front-side bus, is responsible for transferring data between the processor and other components of the computer system.

ii. Here are the advantages of a high-performance internal data bus in a Pentium processor:

Faster data transfer

i. A high-speed internal data bus allows for faster transfer of data between the processor and other system components, such as memory, input/output devices, and peripheral devices.

ii. This results in quicker data access and improved overall system performance.

Increased bandwidth

i. A wider internal data bus can provide a higher bandwidth for data transfer.

ii. This allows for more data to be transferred simultaneously, which is beneficial for tasks that require large amounts of data, such as multimedia processing or data-intensive applications.

Improved system responsiveness

i. The internal data bus plays a crucial role in overall system responsiveness.

ii. By enabling fast and efficient communication between the processor and other components, it ensures smooth operation and reduces delays in data transfer, leading to a more responsive system.

Support for advanced features

i. A robust internal data bus can support advanced features and technologies, such as multiprocessing or multi-core architectures.

ii. These features allow for better utilization of system resources, improved multitasking capabilities, and enhanced performance in demanding computing environments.

iii. Overall, both prefetching and a high-performance internal data bus contribute to the performance and efficiency of Pentium processors, enabling faster data access, improved instruction execution, and enhanced system responsiveness.

3.8 PROGRAMMING MODEL OF 32-BIT VERSION OF X86 FAMILY OF MICROPROCESSORS

Board Exam Question

Q. Explain the programming model of 32 bit version of X86 family of microprocessors.

(March 07, 08, 14,16, Oct. 05, 07,13, 3/4 Marks)

i. The 32-bit version of the x86 family of microprocessors follows a specific programming model that governs how software interacts with the processor.

ii. The programming model defines the registers, memory organization, and instruction set architecture that software developers utilize to write programs for the processor.

iii. The Fig. 3.8.1 shows the programming model for the 32-bit x86 microprocessors.

iv. These are some of the key aspects of the programming model for the 32-bit version of the x86 family of microprocessors.

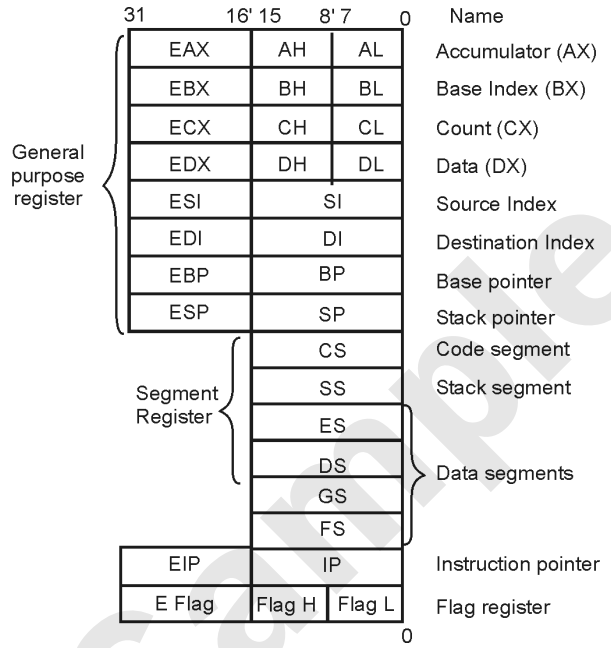

Fig. 3.8.1 : Programming model for the 32-bit x86 microprocessors

v. Understanding this model is essential for software developers to write efficient and compatible code for these processors.

Registers

i. The 32-bit x86 architecture provides several general-purpose registers, including **EAX, EBX, ECX, EDX, ESI, EDI, EBP, and ESP**. These registers are used for various purposes, such as storing data, addressing memory, and holding temporary values during computations.

Memory Organization

i. The 32-bit x86 architecture supports a linear address space of up to 4 GB (2^32 bytes).

ii. This address space is divided into segments, including code segment, data segment, stack segment, and extra segments. The segments are used to manage memory access and provide different regions for storing code and data.

Instruction Set Architecture (ISA)

i. The ISA of the 32-bit x86 microprocessors includes a wide range of instructions for performing arithmetic and logical operations, data movement, control flow, and more.

ii. These instructions are encoded in binary format and can be executed by the processor.

Stack

i. The 32-bit x86 architecture employs a stack to manage function calls, local variables, and return addresses.

ii. The stack grows downward in memory, and the ESP (Extended Stack Pointer) register points to the top of the stack.

Calling Conventions

i. The 32-bit x86 architecture has several calling conventions that define how functions are called and how arguments and return values are passed.

ii. The most common calling convention is the CDECL convention, where arguments are pushed onto the stack in reverse order, and the caller is responsible for cleaning up the stack.

Interrupts and Exceptions

i. The x86 architecture supports interrupts and exceptions, which are mechanisms for handling events and errors during program execution.

ii. When an interrupt or exception occurs, the processor transfers control to a specific interrupt handler or exception handler to handle the event.

Privilege Levels

i. The 32-bit x86 microprocessors support four privilege levels, known as rings, ranging from 0 to 3.

ii. **Ring 0** (also called the kernel mode) has the highest privilege level and is used by the operating system, while rings 1 and 2 are typically reserved for device drivers and privileged software. **Ring 3** (also called the user mode) has the lowest privilege level and is used for user applications.

3.9 FLAG REGISTER (32-BIT) OF X86 FAMILY

Board Exam Question

Q. Draw a neat-labeled diagram of 32-bit flag register of X86 family. **(Oct. 05, 3 Marks)**

The X86 family of processors includes a 32-bit flag register known as the **EFLAGS register**. The EFLAGS register contains various individual flags that indicate the status and control certain aspects of the processor's operation. Flag register of the X86 family is as shown in the Fig. 3.9.1.

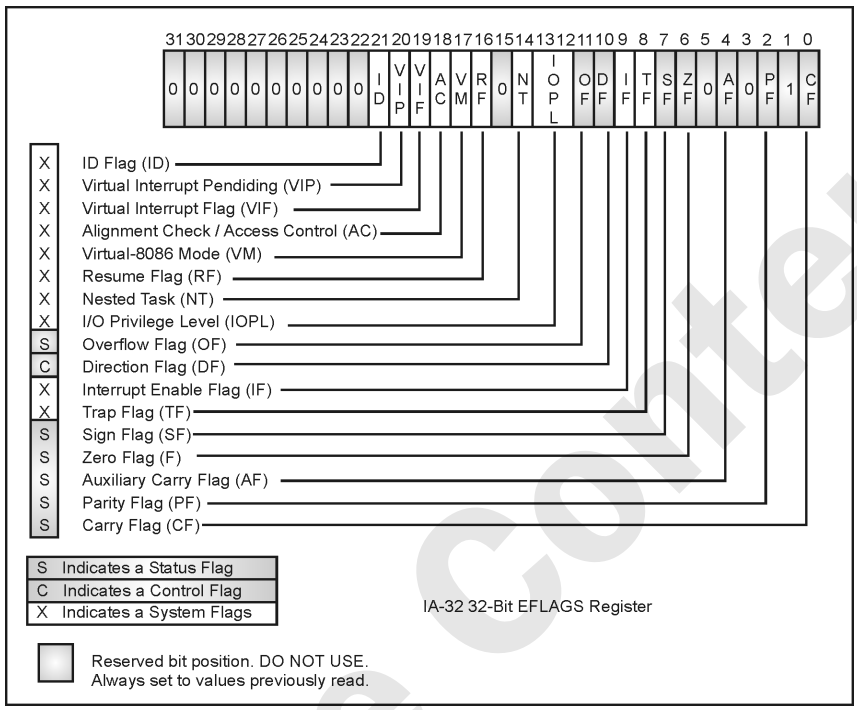

Fig. 3.9.1 : Flag register of the X86 family

Here are some of the commonly used flags in the EFLAGS **register.**

i. **Carry Flag (CF) :** This flag is used for arithmetic operations and indicates if there was a carry or borrow during the operation.

ii. **Parity Flag (PF) :** This flag indicates the parity (even or odd) of the least significant byte of the result.

iii. **Auxiliary Carry Flag (AF) :** This flag is used for binary-coded decimal (BCD) arithmetic operations and indicates a carry or borrow between bits 3 and 4.

iv. **Zero Flag (ZF) :** This flag is set if the result of an operation is zero.

v. **Sign Flag (SF) :** This flag is set if the result of an operation is negative.

vi. **Overflow Flag (OF) :** This flag is set if the result of a signed arithmetic operation overflows.

vii. **Direction Flag (DF) :** This flag is used by string operations to control the direction of data movement (forward or backward).

viii. **Interrupt Flag (IF) :** This flag enables or disables the processor's ability to respond to external interrupts.

ix. **Trap Flag (TF) :** This flag is used for debugging purposes and enables single-step execution of instructions.

x. **Resume Flag (RF) :** This flag is used for debugging purposes and allows the processor to resume execution after handling a debug exception.

IOPL (I/O Privilege level) flag

i. It is a flag found on all IA-32 compatible x86 CPUs. It occupies bits 12 and 13 in the FLAGS register.

ii. In protected mode and long mode, it shows the I/O privilege level of the current program or task. The CPL (Current Privilege Level) (**CPL0, CPL1, CPL2, CPL3**) of the task or program must be less than or equal to the IOPLin order for the task or program to access I/O ports.

iii. The IOPL can be changed using POPF(D) and IRET(D) only when the current privilege level is Ring 0.

iv. Besides IOPL, the I/O Port Permissions in the TSS also take part in determining the ability of a task to access I/O port.

NT Flag

If NT = 1, it indicates that the currently executing task is nested within another task and it has a valid link to caller task i.e., this task is executed using the call instruction.

VM (virtual mode)

i. The VM flag bit selects virtual mode operation in a protected mode system.

ii. A virtual mode system allows multiple DOS memory par-titions that are 1M byte in length to coexist in the memory system. Essentially, this allows the system program to execute multiple DOS programs.

AC (alignment check)

i. The alignment check flag bit activates if a word or double word is addressed on a non-word or non-double word boundary.

ii. Only the 80486SX microprocessor contains the alignment check hit that is primarily used by its companion numeric coprocessor, the 80487SX, for synchronization.

VIF (virtual interrupt flag)

The VIF is a copy of the interrupt flag bit available to the Pentium-Pentium II microprocessors.

VIP (virtual interrupt pending)

i. VIP provides information about a virtual mode interrupt for the Pentium-Pentium II microprocessors.

ii. This is used in multitasking environments to provide the operating system with virtual interrupt flags and interrupt pending information.

ID (identification)

The ID flag indicates that the Pentium-Pentium II microprocessors support the CPUID instruction. The CPUID instruction provides the system with information about the Pentium microprocessor, such as its version number and manufacturer.

3.10 COMPARISON OF X86 FAMILY MICROPROCESSORS

Board Exam Questions

Q. Compare any four attributes of 80286 and Pentium microprocessor.
(March 04,09,12,16,17,19,April 2023, Oct 04,06,09,11,16)

Q. Explain in brief different members of X86 family.
(Oct. 04, 4 Marks)

Table 1.2 : Evolution of Intel's Microprocessors (from the 8086 to the Pentium)

Product	8086	80286	80386	80486	Pentium
Year introduced	1978	1982	1985	1989	1992
Technology	NMOS	NMOS	CMOS	CMOS	BICMOS
Clock rate (MHz)	3-10	10-16	16-33	25-33	60-66
Number of pins	40	68	132	168	273
Number of transistors	29,000	130,000	275,000	1.2 million	3.1 million
Physical memory	1M	16M	4G	4G	4G
Virtual memory	None	1G	64T	64T	64T
Internal data bus	16	16	32	32	32
External data bus	16	16	32	32	64
Address bus	20	24	32	32	32
Data type (bits)	8, 16	8, 16	8, 16, 32	8, 16, 32	8,16, 32

3.11 MULTIPLE CHOICE QUESTIONS

1. The intel 8086 microprocessor is a processor.
   (a) 8 bit (b) 16 bit
   (c) 32 bit (d) 4 bit
   (July 22, 1 Mark)
   ✓ **Ans. : (b)**

2. In 8086 microprocessor, the address bus is bit wide.
   (a) 12 bit (b) 16 bit
   (c) 20 bit (d) 8 bit
   ✓ **Ans. : (c)**

3. The microprocessor can read/write 16 bit data from or to
   (a) Memory (b) I /O device
   (c) processor (d) register
   ✓**Ans. : (a)**

4. The work of EU is
   (a) encoding (b) decoding
   (c) processing (d) calculations
   ✓**Ans. : (b)**

5. The 16-bit flag of 8086 microprocessor is responsible to indicate_____.
   (a) the condition of result of ALU operation
   (b) the condition of memory
   (c) the result of addition
   (d) the result of subtraction ✓**Ans. : (a)**

6. The SP is indicated by
   (a) single pointer (b) stack pointer
   (c) source pointer (d) destination pointer
   ✓**Ans. : (b)**

7. The DS is called as
   (a) data segment
   (b) digital segment
   (c) Divide segment
   (d) decode segment ✓**Ans. : (a)**

8. The BIU contains FIFO register of size_____ bytes
(a) 12 (b) 8 (c) 6 (d) 4
✓**Ans. : (c)**

9. The 1 MB byte of memory can be divided into segment
(a) 1 Kbyte (b) 64 Kbyte
(c) 33 Kbyte (d) 34 Kbyte
✓**Ans. : (b)**

10. The index register is used to hold
(a) memory register (b) offset address
(c) segment memory (d) offset memory
✓**Ans. : (a)**

11. The BP is indicated by
(a) base pointer (b) binary pointer
(c) bit pointer (d) digital pointer
✓**Ans. : (a)**

12. The BIU prefetches the instruction from memory and store them in
(a) Stack (b) memory
(c) register (d) queue ✓**Ans. : (d)**

13. The OF is called as
(a) overflow flag (b) overdue flag
(c) one flag (d) over flag
✓**Ans. : (a)**

14. The CF is known as
(a) carry flag (b) condition flag
(c) common flag (d) single flag
✓**Ans. : (a)**

15. The SF is called as
(a) service flag (b) sign flag
(c) single flag (d) condition flag
✓**Ans. : (b)**

16. Which bus is a bidirectional bus?
(a) address bus
(b) data bus
(c) address bus and data bus
(d) none of the above ✓**Ans. : (b)**

17. The intel 80286 is a _____ microprocessor.
(a) 16 bit (b) 8 bit
(c) 32 bit (d) None of these
(Oct. 05, 1 Mark)
✓**Ans. :(a)**

18. _____ is a 32 bit microprocessor.
(a) 8086 (b) 80386
(c) Intel Pentinum (d) M68000
(Oct. 07, 1 Mark)
✓**Ans. :(b)**

19. Data bus of 80286 MPU is of size _____ .
(a) 8 bit (b) 16 bit
(c) 32 bit (d) 64 bit
(March 15, 1 Mark)
✓**Ans. :(b)**

20. The maximum physical memory can be addressed by80286 microprocessor is _____.
(a) 640 KB (b) 1 MB
(c) 16 MB (d) 4 KB
(March 17, April 23, 1 Mark)
✓**Ans. :(c)**

21. The faulty 32-bit microprocessor from the following is _____.
(a) 8086 (b) 8085
(c) 80386 (d) 80586
(July 17, 1 Mark)
✓**Ans. :(c)**

22. The 8051 micro-controller has instruction set of _____ instructions.
(a) 101 (b) 110
(c) 99 (d) 111
(March 19, 1 Mark)
✓**Ans. :(d)**

23. The instructions available in the 80386 that are not available in its real address mode is
(a) addressing techniques
(b) instructions for protected address mode
(c) instructions for interrupt handling
(d) all of the mentioned ✓**Ans. :(b)**

24. The 16-bit registers are available with their extended size of 32 bits, by adding the registers with a prefix of
(a) X (c) E
(c) 32 (d) XX ✓**Ans. :(b)**
Explanation : A 32 bit register, known as an extended register, is represented by the register name with a prefix of E.

25. In a 32-bit register, ESP, the lower 16-bits of the register can be represented by
(a) LSP
(b) FSP
(c) SP
(d) None of the mentioned ✓**Ans. :(c)**

26. Which is the microprocessor comprises :
(a) Register section (b) One or more ALU
(c) Control unit (d) All of these
✓**Ans. : (d)**

27. What is the store by register?
(a) data (b) operands
(c) memory (d) None of these
✓**Ans. : (a)**

28. Accumulator based microprocessor example are:
(a) Intel 8085 (b) Motorola 6809
(c) a and b (d) None of these
✓**Ans. : (c)**

29. A set of register which contain are:
(a) data
(b) memory addresses
(c) result
(d) all of these
✓**Ans. : (d)**

30. There are primarily two types of register :
(a) general purpose register
(b) dedicated register
(c) a and b
(d) none of these ✓**Ans. : (c)**

31. Name of typical dedicated register is:
(a) PC (b) IR
(c) SP (d) All of these
✓**Ans. : (d)**

32. BCD stands for:
(a) Binary coded decimal
(b) Binary coded decoded
(c) Both a & b
(d) none of these ✓**Ans. : (a)**

33. Which is used to store critical pieces of data during subroutines and interrupts :
(a) Stack (b) Queue
(c) Accumulator (d) Data register
✓**Ans. : (a)**

34. The data in the stack is called:
(a) Pushing data (b) Pushed
(c) Pulling (d) None of these
✓**Ans. : (a)**

35. The external system bus architecture is created using from architecture :
(a) Pascal (b) Dennis Ritchie
(c) Charles Babbage (d) Von Neumann
✓**Ans. : (d)**

36. The processor 80386/80486 and the Pentium processor uses bits address bus :
(a) 16 (b) 32
(c) 36 (d) 64 ✓**Ans. : (b)**

37. Which is not the control bus signal :
(a) READ (b) WRITE
(c) RESET (d) None of these
✓**Ans. : (c)**

38. PROM stands for :
(a) Programmable read-only memory
(b) Programmable read write memory
(c) Programmer read and write memory
(d) None of these ✓**Ans. : (a)**

39. EPROM stands for:
(a) Erasable Programmable read-only memory
(b) Electrically Programmable read write memory
(c) Electrically Programmable read-only memory
(d) None of these ✓**Ans. : (a)**

40. Each memory location has :
(a) Address (b) Contents
(c) Both a and b (d) None of these
✓**Ans. : (c)**

41. Which is the type of microcomputer memory :
(a) Processor memory
(b) Primary memory
(c) Secondary memory
(d) All of these ✓**Ans. : (d)**

42. Secondary memory can store :
(a) Program store code
(b) Compiler
(c) Operating system
(d) All of these ✓**Ans. : (d)**

43. Secondary memory is also called :
(a) Auxiliary (b) Backup store
(c) Both a and b (d) None of these
✓**Ans. : (c)**

44. Customized ROMS are called :
(a) Mask ROM (b) Flash ROM
(c) EPROM (d) None of these
✓**Ans. : (a)**

45. The RAM which is created using bipolar transistors is called :
(a) Dynamic RAM (b) Static RAM
(c) Permanent RAM (d) DDR RAM
✓**Ans. : (b)**

46. Which type of RAM needs regular referred :
(a) Dynamic RAM (b) Static RAM
(c) Permanent RAM (d) SD RAM
✓**Ans. : (a)**

47. Which RAM is created using MOS transistors :
(a) Dynamic RAM (b) Static RAM
(c) Permanent RAM (d) SD RAM
✓**Ans. : (a)**

48. A microprocessor retries instructions from :
(a) Control memory (b) Cache memory
(c) Main memory (d) Virtual memory
✓**Ans. : (c)**

49. The lower red curvy arrow show that CPU places the address extracted from the memory location on the:
(a) Address bus (b) System bus
(c) Control bus (d) Data bus
✓**Ans. : (a)**

50. The CPU sends out a signal to indicate that valid data is available on the data bus :
(a) Read (b) Write
(c) Both a and b (d) None of these
✓**Ans. : (b)**

51. The CPU removes the signal to complete the memory write operation :
(a) Read (b) Write
(c) Both a and b (d) None of these
✓**Ans. : (a)**

52. BIU STAND FOR:
(a) Bus interface unit
(b) Bess interface unit
(c) a and b
(d) None of these ✓**Ans. : (a)**

53. EU STAND FOR:
(a) Execution unit (b) Execute unit
(c) Exchange unit (d) None of these
✓**Ans. : (a)**

54. Which are the four categories of registers:
(a) General- purpose register
(b) Pointer or index registers
(c) Segment registers
(d) Other register
(e) All of these ✓**Ans. : (e)**

55. Eight of the register are known as:
(a) General- purpose register
(b) Pointer or index registers
(c) Segment registers
(d) Other register ✓**Ans. : (a)**

56. The four index register can be used for:
(a) Arithmetic operation
(b) Multipulation operation
(c) Subtraction operation
(d) All of these ✓**Ans. : (a)**

57. IP Stand for :
(a) Instruction pointer
(b) Instruction purpose
(c) Instruction paints
(d) None of these ✓**Ans. : (a)**

58. CS Stand for :
(a) Code segment (b) Coot segment
(c) Cost segment (d) Counter segment
✓**Ans. : (a)**

59. DS Stand for:
(a) Data segment (b) Direct segment
(c) Declare segment (d) Divide segment
✓**Ans. : (a)**

60. Which are the segment:
(a) CS: Code segment
(b) DS: data segment
(c) SS: Stack segment
(d) ES:extra segment
(e) All of these
✓**Ans. : (d)**

61. The acculatator is 16 bit wide and is called :
(a) AX (b) AH
(c) AL (d) DL ✓**Ans. : (a)**

62. How many bits the instruction pointer is wide :
(a) 16 bit (b) 32 bit
(c) 64 bit (d) 128 bit
✓**Ans. : (a)**

63. How many type of addressing in memory:
(a) Logical address (b) Physical address
(c) Both a and b (d) None of these
✓**Ans. : (c)**

64. The size of each segment in 8086 is:
(a) 64 kb (b) 24 kb
(c) 50 kb (d) 16kb ✓**Ans. : (a)**

65. The address of a memory is a 20 bit address for the 8086 microprocessor:
(a) Physical (b) Logical
(c) Both (d) None of these
✓**Ans. : (a)**

66. The pin configuration of 8086 is available in the :
(a) 40 pin (b) 50 pin
(c) 30 pin (d) 20 pin
✓**Ans. : (a)**

67. DIP stand for:
(a) Deal inline package
(b) Dual inline package
(c) Direct inline package
(d) Digital inline package ✓**Ans. : (b)**

68. EA stand for:
(a) Effective address (b) Electrical address
(c) Effect address (d) None of these
✓**Ans. : (a)**

69. BP stand for :
(a) Bit pointer (b) Base pointer
(c) Bus pointer (d) Byte pointer
✓**Ans. : (b)**

70. DI stand for:
(a) Destination index (b) Defect index
(c) Definition index (d) Delete index
✓**Ans. : (a)**

71. SI stand for:
(a) Stand index (b) Source index
(c) Segment index (d) Simple index
✓**Ans. : (b)**

72. ALE stand for:
(a) Address latch enable
(b) Address light enable
(c) Address lower enable
(d) Address last enable ✓**Ans. : (a)**

73. NMI stand for :
(a) Non mask able interrupt
(b) Non mistake interrupt
(c) Both
(d) None of these ✓**Ans. : (a)**

74. _____is the most important segment and it contains the actual assembly language instruction to be executed by the microprocessor:
(a) Data segment (b) Code segment
(c) Stack segment (d) Extra segment
✓**Ans. : (b)**

75. The offset of a particular segment varies from :
(a) 000H to FFFH
(b) 0000H to FFFFH
(c) 00H to FFH
(d) 00000H to FFFFFH
✓**Ans. : (b)**

76. Which are the factor of cache memory :
(a) Architecture of the microprocessor
(b) Properties of the programs being executed
(c) Size organization of the cache
(d) All of these ✓**Ans. : (d)**

77. _____is usually the first level of memory access by the microprocessor :
(a) Cache memory (b) Data memory
(c) Main memory (d) All of these
✓**Ans. : (a)**

78. Which is the small amount of high- speed memory used to work directly with the microprocessor:
(a) Cache (b) Case
(c) Cost (d) Coos ✓**Ans. : (a)**

79. The cache usually gets its data from the whenever the instruction or data is required by the CPU:
(a) Main memory (b) Case memory
(c) Cache memory (d) All of these
✓**Ans. : (a)**

80. Microprocessor reference that are available in the cache are called :
(a) Cache hits (b) Cache line
(c) Cache memory (d) All of these
✓**Ans. : (a)**

81. Microprocessor reference that are not available in the cache are called :
(a) Cache hits (b) Cache line
(c) Cache misses (d) Cache memory
✓**Ans. : (c)**

82. Which causes the microprocessor to immediately terminate its present activity :
(a) RESET signal
(b) INTERUPT signal
(c) Both
(d) None of these ✓**Ans. : (a)**

83. Which is responsible for all the outside world communication by the microprocessor :
(a) BIU (b) PIU
(c) TIU (d) LIU ✓**Ans. : (a)**

84. INTR : it implies the signal :
(a) INTRRUPT REQUEST
(b) INTRRUPT RIGHT
(c) INTRRUPT RONGH
(d) INTRRUPT RESET ✓**Ans. : (a)**

85. Which of the following are the two main components of the CPU?
(a) Control Unit and Registers
(b) Registers and Main Memory
(c) Control unit and ALU
(d) ALU and bus ✓**Ans. : (c)**

…Chapter Ends

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